GAU 2811

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#4 IDS 3-15-01 R Stokes

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/764,242 01/19/01

George Wong

A FILL PATTERN IN KERF AREAS TO PREVENT LOCALIZED NON-UNIFORMITIES OF INSULATING LAYERS AT DIE CORNERS ON SEMICONDUCTOR SUBSTRATES

Grp. Art Unit: 2811

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,663,599 to Lur, "Metal Layout Pattern for Improved Passivation Layer Coverage", teaches a method of forming dummy metal lines at the end of the functional metal lines.

U.S. Patent 5,[illegible] to Michael et al., "Mask Generation Technique for Producing an Integrated Circuit with Optimal Polysilicon Interconnect Layout for Achieving Global Planarization", describes a method utilizing non-operational conductors spaced at a minimum distance from each other to form a regular spaced arrangement of conductors in the die areas for integrated circuits.

U.S. Patent 5,763,955 to Findley et al., "Patterned Filled Layers for Integrated Circuit Manufacturing", describes a method in which polygon-shaped, metal-fill segments (dummy lines) are used to fill the spaces between the functional metal lines on the die areas for the integrated circuit to allow for gloabal planarization on each of the die areas across the substrate.

U.S. Patent 5,618,757 to Boghra et al., "Method for Improving the Manufacturability of the Spin-On Glass Etchback Process", describes a method in which dummy raised areas are formed in the gaps between the active conductive metal lines (traces).

U.S. Patent 5,589,706 to Mitwalsky et al., "Fuse Link Structures through the Addition of Dummy Structures", describes a method of making reliable fuse-link structures with vertical sidewalls by using dummy structures adjacent to the fuse, but the dummy structures do not form part of the fuse structure.

U.S. Patent 5,763,936 to Yamaha et al., "Semiconductor Chip Capable of Supressing Cracks in Insulating Layer", teaches a method of reducing cracking in a thick spin-on-glass film which is used to hermetically seal the chip.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761